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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/725,073 | 12/01/2003 | Eiji Ohta | 09792909-5742 | 2729 |

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SONNENSCHEIN NATH & ROSENTHAL
Sears Tower
Wacker Drive Station
P.O. Box 061080
Chicago, IL 60606-1080

| EXAMINER | |
|---|---|
| WALSH, DANIEL I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2876 | |

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/725,073 | OHTA ET AL. | |
| | Examiner | Art Unit | |
| | Daniel I. Walsh | 2876 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Receipt is acknowledged of the RCE received on 15 August 2005.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 10, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami et al. (US 6,166,911) in view of Ota et al., as cited in the previous Office Action.

Usami et al. teaches an IC module with an IC chip mounted on a substrate having an antenna/coil, and a core layer comprising a plurality of sheet materials having the IC module disposed there between, wherein the sheet materials adjacent to the IC module have a through hole for containing therein the IC chip, formed in a region corresponding to an IC mounted

portion of the module, wherein the plurality of sheet materials comprise at least a pair of inner core sheets adjacent to the module (FIG. 5). Usami et al. teaches the IC is 30 um in thickness (FIG. 1 and 2). Accordingly, it is obvious that the relationship set forth in the claims is satisfied, as the relationship does not specify that any of the variables are required to be non-zero and that a projection height is specifically broad to be read upon.

Usami et al. is silent to a reinforcing plate on the IC mounted surface of the substrate.

Ota et al. teaches a reinforcing plate on an IC mounted portion, as discussed in the previous Office Action.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Usami et al. with those of Ota et al.

One would have been motivated to do this to increase the strength of the card by using a reinforcing plate, as is known in the art.

The limitations of claims 10 and 17 have been discussed above.

3. Claims 1-5, 7-12, and 14-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Ota et al. (JP 2002-163624).

Ota et al teaches an IC card with an IC chip 5 mounted on an insulating substrate 1 having an antenna coil 3, and a chip reinforcing plate (9, 9') provided on at least an IC mounted surface of the insulating substrate, a core layer 13 comprising a plurality of sheet materials 15,16 having an IC module disposed therein. The plurality of sheet materials comprise a pair of inner core sheets 15,16 that are adjacent to the IC module. Though Ota et al. is silent to through holes for the IC module, the examiner notes it is well known and conventional to have such a hole/recess in order to fit the IC module into the core, and therefore such modification is well

known and conventional in the art, as an obvious expedient. For clarification purposes, the Examiner notes that though Ota et al. is silent to through holes/cavities, that FIG. 1 shows an arrangement where an IC ship and reinforcing plates are disposed in what appears to be a holes/cavity (interpreted as a through hole by the Examiner). In FIG. 1, the height of the hole appears to be equal to that of the projections, thus satisfying the relationships set forth in the claims 1-5, 10-12, and 18-20. It is interpreted by the Examiner that upon formation of the card by pressure, that a through hole is created. As the claims do not recite that the through hole is cut before chip placement, that the through hole penetrates certain layers/sheets, Ota et al. is believed to read upon the claimed limitations. Additionally, the Examiner notes that the term "projection" is sufficiently broad. The claims have not recited what the projection is, and the Examiner notes that any reasonable interpretation can be applied by additional art, to meet the broad recitation of a projection.

Re claims 2-5, 11-12, and 18-20 the Examiner notes that as the space is filled with resin/sealant (no gap), the relationships are satisfied.

Re claim 7, display layer 20 is a rewritable display layer.

Re claims 8-9, Ota et al. teaches the limitations (paragraph [0037]+)

Re claims 10-12 and 14-20, the limitations have been discussed above.

4. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ota et al., as discussed above, in view of Saito et al. (JP 11078324).

The teachings of Ota et al. have been discussed above.

Ota et al. is silent to an outer core sheet stacked on at least one of the pair of inner core sheets.

Saito et al. teaches outer core sheets (SOLUTION).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ota et al. with those of Saito et al.

One would have been motivated to do this to increase impact resistance strength and heat resistance/protection.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. The Examiner has cited the new art to Saito for the newly added limitations of claims 6 and 13.

The Examiner notes that the Applicant did not amend independent claim 17, and therefore the rejection of claims 17-20 are repeated.

The Examiner notes that the limitation that the sheets of the core layer comprise inner core sheets adjacent to the IC module, the Examiner has broadly interpreted that the layers 15,16 as inner core sheets adjacent to the module.

The Examiner notes that the limitations of "projection height" is sufficiently broad. There is no explanation of what the projection is of, what direction it is in, etc. The Examiner notes that such a limitation appears sufficiently broad to be potentially be read on by prior art, as what is being projected is not specified, and is left open to broad interpretation.

The Examiner notes that the limitation of the through holes is sufficiently broad to include a hole or recess cut into a substrate/layer, analogous to digging a hole. The claims have

not recited that the through hole passes completely through various layers/sheets, and therefore the prior art is interpreted to read up such limitations.

Finally, the Examiner notes that the mathematical expressions regarding the variables A, B1, C1, etc. are sufficiently broad to be read upon by the prior art because the projection heights have not been specifically defined, the variables have not been required to be non-zero, etc.

### *Additional Remarks*

6. The Examiner notes that Usami et al., as discussed above, teaches that the size of an IC chip is in the range of 30 micrometers.

### *Conclusion*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Haghiri-Tehrani et al. (US 5,851,854), Welling (US 6,283,378), Kim et al. (US 2003/0226901), Melzer et al. (US 6,305,609), Hida et al. (US 4,841,134), Takeda et al. (US JP02004171100), Honda (JP02002197433), Akiyama (JP02000155822), Hoshi (JP411048660), and Iwahashi et al. (JP02001319210), which are drawn toward cards with through holes/multilayered structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel I. Walsh whose telephone number is (571) 272-2409. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel I Walsh
Examiner
Art Unit 2876
12-13-05